CLAIMS:

1. A method of forming integrated circuitry comprising:

forming a silicon nitride comprising layer over a semiconductor substrate;

forming at least one enriched region within the silicon nitride comprising layer, the enriched region comprising Al, Ga or a mixture thereof;

forming a silicon dioxide comprising layer proximate the silicon nitride comprising layer; and

removing the silicon dioxide comprising layer substantially selectively relative to the silicon nitride comprising layer, the at least one enriched region enhancing selectivity to the silicon nitride comprising layer during the removing.

2. The method of claim 1 wherein the silicon nitride comprising layer has an outer surface, the enriched region extending to at least a portion of the outer surface.

3. The method of claim 1 wherein the silicon nitride comprising layer has an outer surface, the enriched region being spaced from the outer surface.

4. The method of claim 1 wherein the enriched region comprises Al.

5. The method of claim 1 wherein the enriched region comprises Ga.

6. The method of claim 1 wherein the enriched region comprises Al and Ga.

7. The method of claim 1 further comprising annealing the silicon nitride comprising layer prior to the removing.

8. The method of claim 1 wherein the silicon dioxide comprising layer is formed on the silicon nitride comprising layer.

9. The method of claim 1 wherein the silicon dioxide comprising layer is substantially undoped.

10. The method of claim 1 wherein the silicon dioxide comprising layer is doped.

11. The method of claim 1 wherein the removing comprises etching.

12. A method of forming integrated circuitry comprising:

forming a silicon nitride comprising layer over a semiconductor substrate;

implanting at least one of Al and Ga into the silicon nitride comprising layer;

forming a silicon dioxide comprising layer proximate the silicon nitride comprising layer; and

removing the silicon dioxide comprising layer substantially selectively relative to the silicon nitride comprising layer, the implanted at least one of Al and Ga enhancing selectivity to the silicon nitride comprising layer during the removing.

13. The method of claim 12 comprising implanting Al.

14. The method of claim 12 comprising implanting Ga.

15. The method of claim 12 wherein the silicon nitride comprising layer has an outer surface, the implanting forming an implanted region which extends to at least a portion of the outer surface.

16. The method of claim 12 wherein the silicon nitride comprising layer has an outer surface, the implanting forming an implanted region which is spaced from the outer surface.

17. A method of forming integrated circuitry comprising:

forming a substantially undoped silicon dioxide comprising layer over a semiconductor substrate;

forming at least one enriched region within the substantially undoped silicon dioxide comprising layer, the enriched region comprising B, Al, Ga or mixtures thereof;

forming a doped silicon dioxide comprising layer proximate the substantially undoped silicon dioxide comprising layer; and

removing the doped silicon dioxide comprising layer substantially selectively relative to the substantially undoped silicon dioxide comprising layer, the at least one enriched region enhancing selectivity to the substantially undoped silicon dioxide comprising layer during the removing.

18. The method of claim 17 wherein the enriched region comprises B.

19. The method of claim 17 wherein the enriched region comprises Al.

20. The method of claim 17 wherein the enriched region comprises Ga.

21. The method of claim 17 wherein the enriched region comprises at least two of B, Al, and Ga.

22. The method of claim 17 wherein the enriched region comprises B, Al, and Ga.

23. The method of claim 17 wherein the doped silicon dioxide is formed on the substantially undoped silicon dioxide.

24. The method of claim 17 wherein the substantially undoped silicon dioxide comprising layer has an outer surface, the enriched region extending to at least a portion of the outer surface.

25. The method of claim 17 wherein the substantially undoped silicon dioxide comprising layer has an outer surface, the enriched region being spaced from the outer surface.

26. The method of claim 17 wherein the removing comprises etching.

27. A method of forming integrated circuitry comprising:

forming a substantially undoped silicon dioxide comprising layer over a semiconductor substrate;

implanting at least one of B, Al, and Ga into the substantially undoped silicon dioxide comprising layer;

forming a doped silicon dioxide comprising layer proximate the substantially undoped silicon dioxide comprising layer; and

removing the doped silicon dioxide comprising layer substantially selectively relative to the substantially undoped silicon dioxide comprising layer, the implanted at least one of B, Al and Ga enhancing selectivity to the substantially undoped silicon dioxide comprising layer during the removing.

28. The method of claim 27 comprising implanting B.

29. The method of claim 27 comprising implanting Al.

30. The method of claim 27 comprising implanting Ga.

31. The method of claim 27 wherein the substantially undoped silicon dioxide comprising layer has an outer surface, the implanting forming an implanted region which extends to at least a portion of the outer surface.

32. The method of claim 27 wherein the substantially undoped silicon dioxide comprising layer has an outer surface, the implanting forming an implanted region which is spaced from the outer surface.

33. A method of forming a contact opening within insulative material to a node location between a pair of conductive device components, comprising:

forming a pair of spaced conductive device components over a semiconductor substrate, each device component having at least one sidewall which faces the other device component of the pair;

forming an insulative material mass over each of said sidewalls, the masses being laterally spaced from one another in a non-contacting relationship, the masses comprising a first insulative material and having a respective lateral outer enriched region comprising B, Al, Ga or mixtures thereof;

forming a second insulative material different from the first insulative material between the insulative material masses; and

etching a contact opening into the second insulative material to a node location between the insulative material masses substantially selectively relative to the insulative material masses, the lateral outer enriched regions enhancing selectivity to the insulative masses during the etching.

34. The method of claim 33 wherein the device components comprise transistor gates.

35. The method of claim 33 wherein the forming of the insulative material masses comprises depositing the first insulative material and anisotropically etching it to form insulative sidewall spacers over each of the sidewalls.

36. The method of claim 33 wherein the enriched region comprises B.

37. The method of claim 33 wherein the enriched region comprises Al.

38. The method of claim 33 wherein the enriched region comprises Ga.

39. The method of claim 33 wherein the first material comprises silicon nitride and the second material comprises silicon dioxide.

40. The method of claim 39 wherein the silicon dioxide is doped.

41. The method of claim 33 wherein the first material comprises substantially undoped silicon dioxide and the second material comprises doped silicon dioxide.

42. The method of claim 33 wherein the insulative masses comprise respective outer surfaces, the enriched regions extending to at least a portion of the respective outer surfaces.

43. A method of forming a contact opening within insulative material to a node location between a pair of conductive device components, comprising:

forming a pair of spaced conductive device components over a semiconductor substrate, each device component having at least one sidewall which faces the other device component of the pair;

forming a silicon nitride comprising layer over the device components and on substrate material between the device components, the silicon nitride comprising layer having a continuous enriched outer region comprising B, Al, Ga or mixtures thereof;

anisotropically etching the silicon nitride comprising layer effective to form insulative spacers over the facing sidewalls of the components, the spacers comprising enriched lateral outer regions of the silicon nitride comprising layer which are elevationally spaced from the substrate material between the device components.

forming an insulative material between the spacers; and

etching a contact opening into the insulative material to a node location between the spacers substantially selectively relative to the spacers, the spacer outer enriched regions enhancing selectivity to the spacers during the etching.

44. The method of claim 43 wherein the insulative masses comprise respective lateral outer surfaces, the enriched regions extending to at least a portion of the respective lateral outer surfaces.

45. The method of claim 43 wherein the insulative material comprises substantially undoped silicon dioxide.

46. The method of claim 43 wherein the insulative material comprises doped silicon dioxide.

47. The method of claim 43 wherein the enriched region comprises B.

48. The method of claim 43 wherein the enriched region comprises Al.

49. The method of claim 43 wherein the enriched region comprises Ga.

50. A method of forming integrated circuitry comprising:

forming a silicon nitride comprising layer over a semiconductor substrate, the silicon nitride comprising layer comprising Al, Ga or a mixture thereof;

forming a silicon dioxide comprising layer proximate the silicon nitride comprising layer; and

removing the silicon dioxide comprising layer substantially selectively relative to the silicon nitride comprising layer, the Al, Ga or a mixture thereof enhancing selectivity to the silicon nitride comprising layer during the removing.

51. The method of claim 50 wherein the Al, Ga or mixture thereof is substantially homogeneously distributed within the silicon nitride comprising layer.

52. The method of claim 50 wherein the silicon nitride comprising layer comprises Al.

53. The method of claim 50 wherein the silicon nitride comprising layer comprises Ga.

54. The method of claim 50 wherein the silicon nitride comprising layer comprises Al and Ga.

55. The method of claim 50 wherein the removing comprises etching.

56. The method of claim 50 wherein the forming of said silicon nitride comprising layer comprises chemical vapor deposition over a previously deposited layer consisting essentially of silicon nitride.

57. A method of forming integrated circuitry comprising:

forming a substantially undoped silicon dioxide comprising layer over a semiconductor substrate, the substantially undoped silicon dioxide comprising layer comprising B, Al, Ga or mixtures thereof;

forming a doped silicon dioxide comprising layer proximate the substantially undoped silicon dioxide comprising layer; and

removing the doped silicon dioxide comprising layer substantially selectively relative to the substantially undoped silicon dioxide comprising layer, the B, Al, Ga or mixtures thereof enhancing selectivity to the substantially undoped silicon dioxide comprising layer during the removing.

58. The method of claim 57 wherein the B, Al, Ga or mixtures thereof is substantially homogeneously distributed within the substantially undoped silicon dioxide comprising layer.

59. The method of claim 57 wherein the substantially undoped silicon dioxide comprising layer comprises B.

60. The method of claim 57 wherein the substantially undoped silicon dioxide comprising layer comprises Al.

61. The method of claim 57 wherein the substantially undoped silicon dioxide comprising layer comprises Ga.

62. The method of claim 57 wherein the removing comprises etching.

63. The method of claim 57 wherein the forming of the substantially undoped silicon dioxide layer comprises chemical vapor deposition of said layer.

64. A method of forming a contact opening within insulative material to a node location between a pair of conductive device components, comprising:

forming a pair of spaced conductive device components over a semiconductor substrate, each device component having at least one sidewall which faces the other device component of the pair;

forming insulative material masses over each of said sidewalls, the masses being laterally spaced from one another in a non-contacting relationship, the masses comprising a first insulative material comprising B, Al, Ga or mixtures thereof;

forming a second insulative material different from the first insulative material between the insulative material masses; and

etching a contact opening to a node location between the insulative material masses substantially selectively relative to the insulative material masses, the B, Al, Ga or mixtures thereof enhancing selectivity to the insulative masses during the etching.

65. The method of claim 64 wherein the B, Al, Ga or mixtures thereof is substantially homogeneously distributed within the insulative material masses.

66. The method of claim 64 wherein the insulative masses comprise B.

67. The method of claim 64 wherein the insulative masses comprise Al.

68. The method of claim 64 wherein the insulative masses comprise Ga.

69. Integrated circuitry comprising:

a pair of spaced conductive device components received over a substrate, and at least partially defining a node location therebetween, each device component having at least one sidewall which faces the other device component of the pair;

an insulative material mass received over each of said sidewalls, the masses being laterally spaced from one another in a non-contacting relationship, the masses comprising a first insulative material comprising B, Al, Ga or mixtures thereof; and

a conductive contact received between the insulative material masses in electrical connection with the node location.

70. The integrated circuitry of claim 69 wherein the B, Al, Ga or mixtures thereof is substantially homogeneously distributed within the insulative material masses.

71. The integrated circuitry of claim 69 wherein the enriched region comprises B.

72. The integrated circuitry of claim 69 wherein the enriched region comprises Al.

73. The integrated circuitry of claim 69 wherein the enriched region comprises Ga.

74. The integrated circuitry of claim 69 wherein the enriched region comprises at least two of B, Al, and Ga.

75. The integrated circuitry of claim 69 wherein the enriched region comprises B, Al, and Ga.

76. Integrated circuitry comprising:

a pair of spaced conductive device components received over a substrate, and at least partially defining a node location therebetween, each device component having at least one sidewall which faces the other device component of the pair;

an insulative material mass received over each of said sidewalls, the masses being laterally spaced from one another in a non-contacting relationship, the masses comprising a first insulative material and having a respective lateral outer enriched region comprising B, Al, Ga or mixtures thereof; and

a conductive contact received between the insulative material masses in electrical connection with the node location.

77. The integrated circuitry of claim 76 wherein the device components comprise field effect transistor gates.

78. The integrated circuitry of claim 76 wherein the insulative material masses comprise anisotropically etched sidewall spacers.

79. The integrated circuitry of claim 76 wherein the insulative masses comprise bases and tops, the bases being wider than the tops.

80. The integrated circuitry of claim 76 wherein the insulative material masses have lateral outer surfaces, the outer enriched regions extending to at least a portion of the lateral outer surfaces.

81. The integrated circuitry of claim 76 wherein the first insulative material comprises substantially undoped silicon dioxide.

82. The integrated circuitry of claim 76 wherein the first insulative material comprises silicon nitride.

83. The integrated circuitry of claim 76 wherein the conductive contact is received on the insulative material masses.

84. The integrated circuitry of claim 76 wherein the enriched region comprises B.

85. The integrated circuitry of claim 76 wherein the enriched region comprises Al.

86. The integrated circuitry of claim 76 wherein the enriched region comprises Ga.

87. The integrated circuitry of claim 76 wherein the enriched region comprises at least two of B, Al, and Ga.

88. The integrated circuitry of claim 76 wherein the enriched region comprises B, Al, and Ga.